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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/640,118	08/16/2000	G. Glenn Henry	CNTR:1356	4572

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EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	3

DATE MAILED: 09/09/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/640,118	Applicant(s) HENRY ET AL.	
	Examiner Aimee J Li	Art Unit 2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 August 2000 and 24 November 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 August 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-24 have been considered.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Change of Address as received on 24 November 2000.

Drawings

3. Figures 1 and 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

5. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 18-21 and 23-24 are rejected under 35 U.S.C. 102(b) as being taught by Richter et al., U.S. Patent Number 5,481,684 (herein referred to as Richter).

8. Referring to claim 18, Richter has taught a microprocessor for executing micro instructions directly from memory, the microprocessor comprising:

a. Translation logic, for receiving macro instructions from the memory, and for decoding said macro instructions into corresponding micro instructions for execution by the microprocessor (Richter Abstract, lines 13-22; column 1, lines 62-67; column 2, lines 13-43; column 3, lines 16-40; column 5, lines 1-14; column 5, line 55 to column 6, line 14; column 10, line 55 to column 11, line 19; column 11, lines 24-39; and Figure 5);

b. Mode detection logic, coupled to said translation logic, for detecting bypass macro instructions, and for directing the microprocessor to execute the micro instructions directly from the memory rather than via said translation logic (Richter Abstract, lines 13-22; column 1, lines 62-67; column 2, lines 13-43; column 3, lines 16-40; column 5, lines 1-14; column 5, line 55 to column 6, line 14; column 10, line 55 to column 11, line 19; column 11, lines 24-39; and Figure 5), said bypass macro instructions comprising:

i. A native branch macro instruction, directing that program control be transferred to a target address (Richter Abstract, lines 13-22; column 1, lines 62-67; column 2, lines 13-43; column 3, lines 16-40; column 5, lines 1-14; column 5, line 55 to column 6, line 14; column 10, line 55 to column 11, line 19; column 11, lines 24-39; and Figure 5); and

ii. A native branch return macro instruction, directing that program control be transferred to a return address (Richter column 3, lines 16-40; column 5, lines 1-14; and column 5, line 55 to column 6, line 14); and

iii. An instruction router, coupled to said mode detection logic, for receiving the micro instructions, and for routing the micro instructions to execution logic, thereby bypassing said translation logic (Richter Abstract, lines 13-22; column 1, lines 62-67; column 2, lines 13-43; column 3, lines 16-40; column 5, lines 1-14; column 5, line 55 to column 6, line 14; column 10, line 55 to column 11, line 19; column 11, lines 24-39; and Figure 5).

9. Referring to claim 19, Richter has taught wherein said mode detection logic, upon execution of said native branch macro instruction, directs said translation logic to cease decoding said macro instructions (Richter column 3, lines 16-40; column 5, lines 1-14; and column 5, line 55 to column 6, line14).

10. Referring to claim 20, Richter has taught wherein said target address designates a location in the memory within which a first one of the micro instructions resides (Richter Abstract, lines 13-22; column 1, lines 62-67; column 2, lines 13-43; column 3, lines 16-40; column 5, lines 1-14; column 5, line 55 to column 6, line 14; column 10, line 55 to column 11, line 19; column 11, lines 24-39; and Figure 5).

11. Referring to claim 21, Richter has taught where said target address is provided in an architectural register (Richter column 3, lines 16-40; column 4, line 53 to column 5, line 14; and column 5, line 55 to column 6, line 14). In regards to Richter, the address must be stored

somewhere and it is well-known that, in x86, operations, such as adding addresses, are mainly done from register to register.

12. Referring to claim 23, Richter has taught wherein said mode detection logic, upon execution of said native branch return macro instruction, directs said translation logic to resume decoding said macro instructions (Richter column 3, lines 16-40; column 5, lines 1-14; and column 5, line 55 to column 6, line 14).

13. Referring to claim 24, Richter has taught wherein said return address designates a next macro instruction, said next macro instruction being one of said macro instructions (Richter column 3, lines 16-40; column 5, lines 1-14; and column 5, line 55 to column 6, line 14).

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claims 1-17 and 22are rejected under 35 U.S.C. 103(a) as being unpatentable over Richter et al., U.S. Patent Number 5,481,684 (herein referred to as Richter) in view of Blomgren et al., U.S. Patent Number 5,781,750 (herein referred to as Blomgren).

16. Referring to claim 1, Richter has taught an apparatus in a microprocessor for executing programmed native instructions that are provided directly to the microprocessor, the apparatus comprising:

a. Instruction translation logic, configured to retrieve macro instructions and configured to decode each of said macro instructions into associated native

instructions for execution by the microprocessor (Richter Abstract, lines 13-22; column 1, lines 62-67; column 2, lines 13-43; column 3, lines 16-40; column 10, line 55 to column 11, line 19; column 11, lines 24-39; and Figure 5); and

b. Bypass logic, coupled to said instruction translation logic, configured to disable said instruction translation logic, and configured to provide the programmed native instructions for execution by the microprocessor, thereby bypassing said instruction translation logic (Richter Abstract, lines 13-22; column 1, lines 62-67; column 2, lines 13-43; column 3, lines 16-40; column 5, lines 1-14; column 5, line 55 to column 6, line 14; column 10, line 55 to column 11, line 19; column 11, lines 24-39; and Figure 5).

17. Richter has not explicitly taught an external instruction bus. Blomgren has taught an external instruction bus (Blomgren column 2, lines 8-9). Richter has incorporated Blomgren by reference (Richter column 1, lines 48-54 and column 3, lines 2-5). In regards to Blomgren, in order for the instruction in memory to be fetched there must be an external bus to transport the data over. A person of ordinary skill at the time the invention was made would have recognized that the instruction must have a means, in this case an external bus, to travel through in order to be transported from memory to the fetcher. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the external bus of Blomgren in Richter so the data will be transported from memory.

18. Referring to claim 2, Richter has not explicitly taught wherein the programmed native instructions are provided from a memory to the external instruction bus. Blomgren has taught wherein the programmed native instructions are provided from a memory to the external

instruction bus (Blomgren column 2, lines 8-9). Richter has incorporated Blomgren by reference (Richter column 1, lines 48-54 and column 3, lines 2-5). In regards to Blomgren, in order for the instruction in memory to be fetched there must be an external bus to transport the data over. A person of ordinary skill at the time the invention was made would have recognized that the instruction must have a means, in this case an external bus, to travel through in order to be transported from memory to the fetcher. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the external bus of Blomgren in Richter so the data will be transported from memory.

19. Referring to claim 3, Richter has taught wherein execution of a native branch macro instruction causes the microprocessor to transfer program control to the programmed native instructions (Richter Abstract, lines 13-22; column 1, lines 62-67; column 2, lines 13-43; column 3, lines 16-40; column 5, lines 1-14; column 5, line 55 to column 6, line 14; column 10, line 55 to column 11, line 19; column 11, lines 24-39; and Figure 5).

20. Referring to claim 4, Richter has taught mode detection logic, configured to detect said native branch macro instruction within a macro instruction sequence that is provided to said instruction translation logic (Richter column 3, lines 16-40; column 5, lines 1-14; and column 5, line 55 to column 6, line 14), wherein, upon detection of said native branch macro instruction, said mode detection logic directs said instruction translation logic to cease decoding said macro instruction sequence following decoding of said native branch macro instruction (Richter column 3, lines 16-40; column 5, lines 1-14; and column 5, line 55 to column 6, line 14).

21. Referring to claim 5, Richter has taught wherein, said instruction translation logic decodes said native branch macro instruction into a native branch native instruction, and wherein

said native branch native instruction directs the microprocessor to transfer program control to a native branch target address (Richter column 3, lines 16-40; column 5, lines 1-14; and column 5, line 55 to column 6, line 14).

22. Referring to claim 6, Richter has taught where said native branch target address is provided in an architectural register (Richter column 3, lines 16-40; column 4, line 53 to column 5, line 14; and column 5, line 55 to column 6, line 14). In regards to Richter, the address must be stored somewhere and it is well-known that, in x86, operations, such as adding addresses, are mainly done from register to register.

23. Referring to claim 7, Richter has taught a native instruction router, coupled to said mode detection logic, configured to receive the programmed native instructions, and configured to route the programmed native instructions to a native instruction bus (Richter Abstract, lines 13-22; column 1, lines 62-67; column 2, lines 13-43; column 3, lines 16-40; column 10, line 55 to column 11, line 19; column 11, lines 24-39; and Figure 5).

24. Referring to claim 8, Richter has taught wherein, said mode detection logic is also configured to detect a native branch return macro instruction, said native branch return macro instruction following the programmed native instructions, wherein, upon detection of said native branch return macro instruction, said mode detection logic directs said instruction translation logic to resume decoding said macro instruction sequence (Richter column 3, lines 16-40; column 5, lines 1-14; and column 5, line 55 to column 6, line 14).

25. Referring to claim 9, Richter has taught wherein said instruction translation logic decodes said native branch return macro instruction into a native branch return native instruction, and wherein said native branch return native instruction directs the microprocessor to transfer

program control to a return address (Richter column 3, lines 16-40; column 5, lines 1-14; and column 5, line 55 to column 6, line 14).

26. Referring to claim 10, Richter has taught wherein said return address designates a next macro instruction, said next macro instruction being within said macro instruction sequence and following said native branch macro instruction (Richter column 3, lines 16-40; column 5, lines 1-14; and column 5, line 55 to column 6, line 14).

27. Referring to claim 11, Richter has taught an apparatus comprising:

a. A translator, for receiving macro instructions from a macro instruction bus, and for translating each of said macro instructions into associated micro instructions, said associated micro instructions being provided to the execution logic via a micro instruction bus (Richter Abstract, lines 13-22; column 1, lines 62-67; column 2, lines 13-43; column 3, lines 16-40; column 5, lines 1-14; column 5, line 55 to column 6, line 14; column 10, line 55 to column 11, line 19; column 11, lines 24-39; and Figure 5); and

b. Bypass logic, coupled to said translator, for routing the micro instruction to the execution logic (Richter Abstract, lines 13-22; column 1, lines 62-67; column 2, lines 13-43; column 3, lines 16-40; column 5, lines 1-14; column 5, line 55 to column 6, line 14; column 10, line 55 to column 11, line 19; column 11, lines 24-39; and Figure 5), said bypass logic comprising:

i. A mode detector (Richter column 3, lines 16-40; column 5, lines 1-14; and column 5, line 55 to column 6, line 14), for detecting a native branch macro instruction, and for directing that said translator cease instruction

translation (Richter column 3, lines 16-40; column 5, lines 1-14; and column 5, line 55 to column 6, line 14); and

ii. A native instruction routing logic, coupled to said mode detector, for receiving said micro instruction from said macro instruction bus, and for providing said micro instruction to said micro instruction bus, thereby circumventing said translator (Richter Abstract, lines 13-22; column 1, lines 62-67; column 2, lines 13-43; column 3, lines 16-40; column 5, lines 1-14; column 5, line 55 to column 6, line 14; column 10, line 55 to column 11, line 19; column 11, lines 24-39; and Figure 5).

28. Richter has not explicitly taught an external instruction bus. Blomgren has taught an external instruction bus (Blomgren column 2, lines 8-9). Richter has incorporated Blomgren by reference (Richter column 1, lines 48-54 and column 3, lines 2-5). In regards to Blomgren, in order for the instruction in memory to be fetched there must be an external bus to transport the data over. A person of ordinary skill at the time the invention was made would have recognized that the instruction must have a means, in this case an external bus, to travel through in order to be transported from memory to the fetcher. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the external bus of Blomgren in Richter so the data will be transported from memory.

29. Referring to claim 12, Richter has not explicitly taught wherein the external instruction bus typically provides said macro instructions to the microprocessor. Blomgren has taught wherein the external instruction bus typically provides said macro instructions to the microprocessor (Blomgren column 2, lines 8-9). Richter has incorporated Blomgren by

reference (Richter column 1, lines 48-54 and column 3, lines 2-5). In regards to Blomgren, in order for the instruction in memory to be fetched there must be an external bus to transport the data over. A person of ordinary skill at the time the invention was made would have recognized that the instruction must have a means, in this case an external bus, to travel through in order to be transported from memory to the fetcher. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the external bus of Blomgren in Richter so the data will be transported from memory.

30. Referring to claim 13, Richter has taught wherein the execution logic executes said native branch macro instruction by transferring program control to a memory address containing the micro instruction (Richter Abstract, lines 13-22; column 1, lines 62-67; column 2, lines 13-43; column 3, lines 16-40; column 5, lines 1-14; column 5, line 55 to column 6, line 14; column 10, line 55 to column 11, line 19; column 11, lines 24-39; and Figure 5).

31. Referring to claim 14, Richter has taught wherein said memory address is provided in an architectural register (Richter column 3, lines 16-40; column 4, line 53 to column 5, line 14; and column 5, line 55 to column 6, line 14). In regards to Richter, the address must be stored somewhere and it is well-known that, in x86, operations, such as adding addresses, are mainly done from register to register.

32. Referring to claim 15, Richter has taught wherein, said mode detector is configured to detect a native branch return macro instruction, wherein, upon detection of said native branch return macro instruction, said mode detection logic directs said translator to resume instruction translation (Richter column 3, lines 16-40; column 5, lines 1-14; and column 5, line 55 to column 6, line 14).

33. Referring to claim 16, Richter has taught wherein the execution logic executes said native branch return macro instruction by transferring program control to a return memory address (Richter column 3, lines 16-40; column 5, lines 1-14; and column 5, line 55 to column 6, line 14).

34. Referring to claim 17, Richter has taught wherein said return memory address contains a next macro instruction (Richter column 3, lines 16-40; column 5, lines 1-14; and column 5, line 55 to column 6, line 14).

35. Referring to claim 23, Richter has not explicitly taught wherein said instruction router routes the micro instructions from a macro instruction bus to a micro instruction bus. Blomgren has taught wherein said instruction router routes the micro instructions from a macro instruction bus to a micro instruction bus (Blomgren column 2, lines 8-9). Richter has incorporated Blomgren by reference (Richter column 1, lines 48-54 and column 3, lines 2-5). In regards to Blomgren, in order for the instruction in memory to be fetched there must be buses to transport the data over. A person of ordinary skill at the time the invention was made would have recognized that the instruction must have a means, in this case buses, to travel through in order to be transported from memory to the decoder. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the external bus of Blomgren in Richter so the data will be transported from memory.

Conclusion

36. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by

the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

a. Boggs et al., U.S. Patent Number 5,581,717, has taught a macro instruction translator which generates micro branch data.

b. Henry et al., U.S. Patent Number 5,812,913, has taught a translator that provides micro code for particular macro instructions.

c. Hammond et al., U.S. Patent Number 5,638,525, has taught a multiple instruction set decoder.

d. Henry et al., U.S. Patent Number 5,638,525, has taught a translator with links to a micro code ROM.

e. Parker et al., U.S. Patent Number 6,041,403, has taught a translator and bypassing the translator to a micro code unit.

37. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (703) 305-7596. The examiner can normally be reached on M-T 7:30am-5:00pm.

38. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

39. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Aimee J. Li
Examiner
Art Unit 2183

September 8, 2003

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
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